

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Sadanand V. Deshpande, et al.

Examiner: Edward Joseph Wojciechowicz

Serial No: 10/751,831

Art unit: 2815

Filed: January 5, 2004

Docket: FIS920030078US2 (16422A)

Title: STI STRESS MODIFICATION BY
NITROGEN PLASMA TREATMENT
FOR IMPROVING PERFORMANCE
IN SMALL WIDTH DEVICES

Dated: October 1, 2007

Confirm. No.: 3568

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

DECLARATION PURSUANT TO 37 C.F.R. §1.131

Sir:

We, Sadanand V. Deshpande, Bruce B. Doris, Werner Rausch, and James A. Slinkman, hereby declare:

1. that we are co-inventors of the subject matter described and claimed in the above-identified patent application;

2. that prior to April 25, 2003, which is the filing date of U.S. Patent Application Publication No. 2004/0212035 to Yeo et al. ("Yeo et al."), we have conceived and reduced to practice a semiconductor structure comprising: a first semiconductor active area having, and laterally surrounded by, a first sidewall and located in a semiconductor substrate; a first trench isolation region laterally abutting the first sidewall and surrounding the first semiconductor active area and comprising silicon oxide, wherein the first sidewall does not contact any nitride liner; a second semiconductor active area having, and laterally surrounded by, a second sidewall

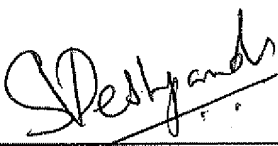
and located in the semiconductor substrate; a nitride liner laterally abutting the second sidewall; and a second trench isolation region laterally abutting the nitride liner and surrounding the second semiconductor active area and comprising silicon oxide;

3. that prior to April 25, 2003, which is the filing date of U.S. Patent Application Publication No. 2004/0212035 to Yeo et al. ("Yeo et al."), we have conceived and reduced to practice a semiconductor structure comprising: a trench isolation region located in a semiconductor substrate; a first semiconductor active area having, and laterally surrounded by, a first sidewall that laterally abuts the trench isolation region and located in the semiconductor substrate, wherein the first sidewall does not contact any nitride liner; a second semiconductor active area having, and laterally surrounded by, a second sidewall and located in the semiconductor substrate; and a nitride liner laterally abutting the second sidewall and the trench isolation region;

4. that as evidence of the conception and reduction to practice of the claimed semiconductor structures referred to in paragraph 2 and 3 prior to the filing date of Yeo et al., annexed hereto is Exhibit A. Exhibit A is a true reprint in PDF format of IBM Invention Disclosure FIS8-2003-0306, which was created prior to April 25, 2004. Exhibit A includes a Main Idea section for the Invention Disclosure, which describes the semiconductor structures that are recited in Claim 21 and Claim 32 of the present application. All names and dates have been redacted in the preparation of this Declaration; and

5. that all statements made herein of our own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that such willful false statements may jeopardize the validity or enforceability of the patent.

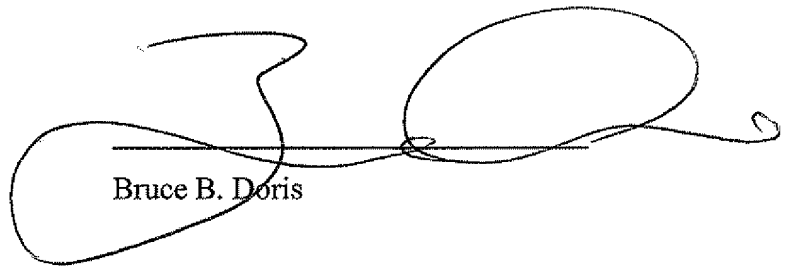
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Sadanand V. Deshpande

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Dated

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Dated



Bruce B. Doris

Werner Rausch

James A. Slinkman

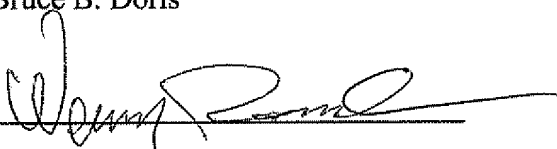
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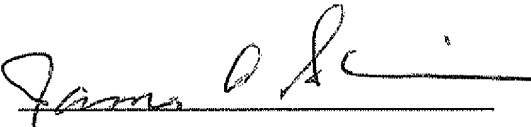
Bruce B. Doris

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Werner Rausch

9/14/2007

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James A. Slinkman